CLAIMS

1. In a multiprocessor system, including at least two processors, and a cache coherency controller, coupled to address concentration devices, a method operable in said cache coherency controller for improving coherent data transfers comprising the steps of:

initiating a first memory transaction request command from said master processor or said cache coherency controller to a first processor of said multiple processors;

determining, within said cache coherency controller, priority receipt status of a next memory transaction request from a subsequent processor or the cache coherency controller through high speed busses;

expanding snoop responses and accumulated snoop responses to provide a coherency action for all cacheline requests utilizing a burst command; and

forwarding said transaction requests from said master or said controller to a solitary global serialization device, said serialization device further comprising a multiple cacheline request indicator.

2. The method of Claim 1 wherein the step of determining the precedence of the priority receipt includes the steps of:

associating a memory transaction request with a unique identifying tag, said tag forwarded to said serialization device, and wherein the step of deploying a first request command includes the step of:

broadcasting the first command and subsequent commands as reflected commands to a plurality of devices.

3. The method of Claim 1 wherein said burst operation occurs on a coherent processor bus comprising the steps of:

grouping multiple and sequential coherent transfers into a single coherent subsequent burst operation on said processor bus; and

determining occurrence of the burst operation;

timing said burst operation;

snooping said burst operation;

concentrating all addresses of said snoop replies; and

broadcasting an agglomerated response of said snoop relies to a plurality of device entities.

4. The method of Claim 3 wherein said determining said occurrence of said burst operation comprises detecting an indication that a plurality of cachelines is requested.

5. The method of Claim 3 wherein said snooping said burst operation comprises separating said burst operation into multiple cacheline requests on a bus.

6. The method of Claim 1 wherein said snooping said burst operation comprises at least a bus and at least a cache directly supporting a burst operation.

7. The method of Claim 6 wherein the total number of indicia comprising said agglomerated burst operation results in a decrease in coherency indicia traffic.

8. The method of Claim 4 wherein said processor support of coherency is greater than a single cacheline.

9. The method of Claim 3 wherein the broadcast of said burst transfer is between pluralities of processors.

10. The method of Claim 4 wherein said determining is a first-in first-out queue determination and wherein the step of queuing said cachelines includes the step of:

determining whether a previous cacheline request corresponding to said processor is already present in said queue; and

queuing said cacheline request in response to a determination that said cacheline request is not already present in said first-in first-out queue.

11. The method of Claim 3 wherein accumulated snoop responses agglomerate as a combined response only on notification of individual responses of said entities within said processors.

12. A computer program product for authenticating code in a computer system, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer code for determining memory transaction requests from a master controller or cache coherency controller;

computer code for verifying memory transaction requests;

computer code for verifying memory transaction request responses;

computer code for agglomerating transaction responses from a plurality of snoop contentions and bus request; and

computer code for initiating a single combined burst operation command.

13. A computer program for providing improved burst transfers

on a coherent bus in a computer system, the burst transfer including a computer program comprising:

computer code for determining device snoops;

computer code for agglomerating a combined response from snoop contentions and bus requests;

computer code for concentrating addresses of responses from processors and devices;

computer code for broadcasting commands to devices from an agglomerated response; and

computer code for determining a resource conflict and issuing a command to the original initiator of the command for reissuance of the command.